BJ8F301A

FAQ

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REV.		
V1.0		2014-07-24
V1.1	FAQ	2014-08-11
V1.2	GPIO P3.4 FAQ	2014-08-21
V1.3	SARADC FAQ	2014-11-07
V1.4	1 JTAG OPTION FAQ 2 STM8 FAQ	2015-03-26
V1.5	1 / IO	2015-09-29
V1.6	1.6 2.6 2.7 2.8 3.3 4.3 5.1 5.2	2015-10-26
V1.7	3.4 AD 8	2016-01-25
V1.8	4.2 ” ”	2016-05-10

1 BJ-Link300

BJ8F301A JTAG BJ-Link300 BJ8F301A
DMA JTAG BJ-Link300
JTAG

1.1 JTAG

LVR WDT JTAG
LVR LVR JTAG

JTAG
JTAG P0.0 RST BJ-Link300 RST

50ms

1.2 JTAG IDLE STOP

IDLE STOP CPU JTAG JTAG
IDLE STOP
RST BJ-Link300 RST IDLE
STOP 50ms

1.3 IDLE STOP

JTAG
run
IDLE STOP JTAG 1.2
RST BJ-link300 RST

1.4 DMA JTAG

BJ8F301A DMA DMA CPU JTAG DMA
DMA

1.5 JTAG OPTION

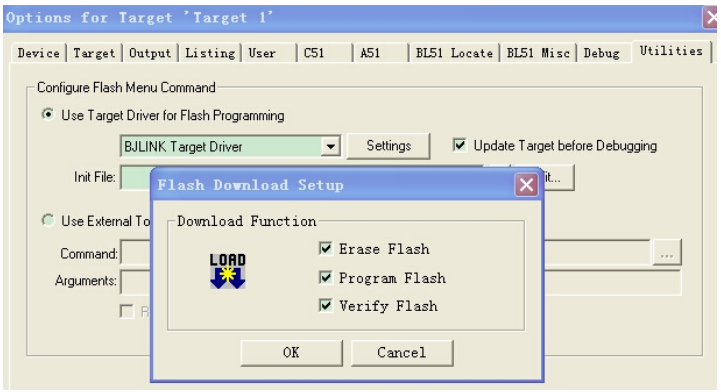
OPTION 1 2

1.6 JTAG PC

1 

2 **“ $NOMOD51 ”**

3 DownLoad , **Load** IC



4 DEBUG LOAD HEX LOAD
LOAD DEBUG DEBUG DEBUG
PC
ICP HEX DEBUG

2

2.1 2 PWM /

PWMx PWMxN / 16Bit xxFFh 8

/ T2PWMxRE T2PWMxMV T2PWMDZ
/ xxFFh 8 / 1
T2PWM1REH=10h T2PWM1REL=20h T2PWM1MV=21h
0FFFh 0FFEh T2PWM1RE T2PWM1MV
T2PWMDZ

2.2

PWM T1PWMxRE
T2PWMxFE T1PWMxRE
T1PWMxRE
PWM
PWM

2.3 PWM

/ /
T1RELR 65535 2 / 0 T2PWMCA

2.4 2 PWM

T2PWM
PWM_CKOEN ; PWMEN ( )
IO

```
T2PWMCON = 0x00;
T2SR = 0x01;
```

2.5 2 PWM

PWM T2 T2
T2CCEN

2.6 PWM

PWM PWM PWM PWM
PWM
PWM PWM

2.7 PWM

PWM PWM PWM PWM
PWM
PWM PWM

2.8 PWM

PWM PWM PWM PWM
PWM PWM PWM
PWM
PWM PWM

3 SAR ADC

3.1 ADC DMA

ADC DMA CPU
DMA CPU DMA CPU DMA
CPU
DMA
DMA

3.2 SARADC

BJ8F301A SAR ADC DRDY AD
DRDY 1 6 NOP
AD

3.3 SARADC AD

1 AD AD
2 **28 NOP** IO AD
3 ADCON1 AD **28 NOP** AD
4 **DRDY 1 6 NOP** **AD** **3.2**
4 AD

3.4 SARADC

1 Vref ADEN

2 2.44V “ ”
WCK CPUCLK, 2.44V WCK IRC ECK

```
/*****************************************************************************
* Function    :  Enable_VREFP_244V
* Description:              2.44V
* Input       :  None
* Output      :  None
*****************************************************************************/
void Enable_VREFP_244V(void )
{
    ANACON1&=0xfd; //      WCK
    CLKSEL |= 0x01;  //       WCK
    _nop_();
    _nop_();
    _nop_();
```

```
    _nop_();
    AD_AMPCON = VREFP_244V; //          Vref
    _nop_();          //delay 100us
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    CLKSEL &= 0xfe; //          ICK
    _nop_();          //      4    NOP
    _nop_();
    _nop_();
    _nop_();
}
```

4 GPIO

4.1 P3.1 P3.4 GPIO

P3.1 P3.4 GPIO P3OE[1] P3.1 P3.4

,

4.2 IO Px[8:0] x=0~3

3 301 302. IO mov

IO IO

IO IO MOV

IO ANL IO

IO IO IO

4- 1 “ - - ”

ANL direct,A		0x52	2	3
ANL direct,#data		0x53	3	4
ORL direct,A		0x42	2	3
ORL direct,#data		0x43	3	4
XRL direct,A		0x62	2	3
XRL direct,#data		0x63	3	4
JBC bit, rel		0x10	3	4
CPL bit		0xB2	2	3
INC direct		0x05	2	3
INC @Ri		0x06-0x07	1	3
DEC direct		0x15	2	3
DEC @Ri		0x16-0x17	1	3
DJNZ direct,rel		0xD5	3	4
MOV bit,C		0x92	2	3
CLR bit		0xC2	2	3
SETB bit		0xD2	2	3

4.3 JTAG P30-P33 IO

JTAG PWM_CKOEN JTAGEN=0

JTAG KEIL ICP

KEIL ICP JTAGEN=1 1

KEIL

5 IIC

5.1 24C02

1 “ + ” 0X40
, , ACK AA=0 I2CF
ACK AA=1 I2CF
24C02
2 I2CF=1 I2CDAT
3 0X50 0x50

5.2 IIC

IIC

6

6.1 ICK ECK

ECK ms 32.768KHz 500ms
ICK ECK ECKSTOPF 1 ECKSTOPF 0
ECK

7

7.1 Timer2

Timer2 TF2 IRCON IRCON
clr TF2 TF2 IRCON[4:0]
TF2 IRCON
Bit TF2 mov IRCON, #0x00

7.2 / IO

I/O

1 EXxIEN IO P

IO EXx=0/1
2 IO I/O 1 1 EXxIEN
IO EXxIEN

8

8.1

1 “ ” Stop WCK CPUCLK, WCK stop
WCK IRC ECK

```
/*****************************************************************************
* Function    :  Enter_Stop
* Description:        STOP
* Input       :  None
* Output      :  None
*****************************************************************************/
void Enter_Stop(void )
{
    ANACON1&=0xfd; //      WCK
    CLKSEL |= 0x01;  //        WCK
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    PCON = 0x02;
    //                  4   NOP
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    _nop_();
    CLKSEL &= 0xfe; //        ICK
    _nop_();            //    4   NOP
    _nop_();
    _nop_();
    _nop_();
}
```

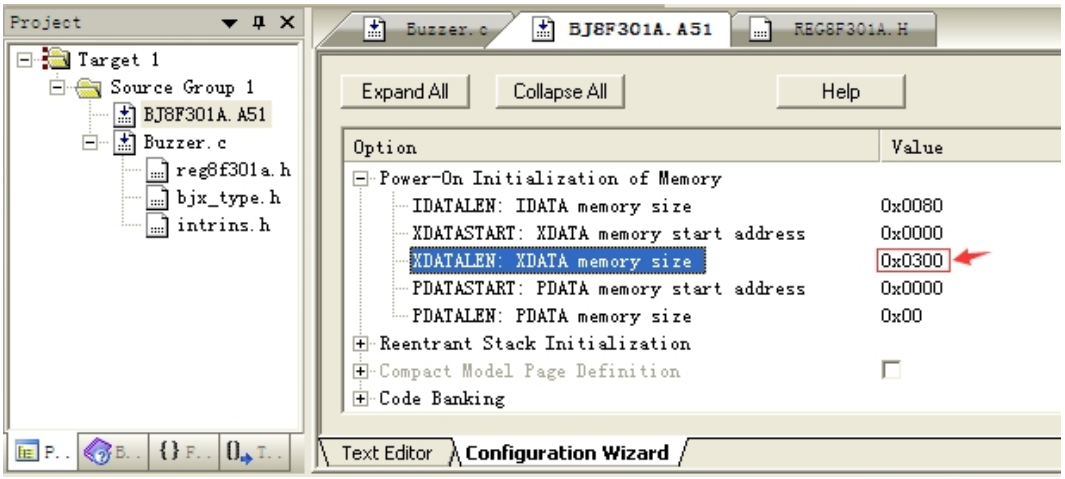
9

9.1 STM8 RAM

ST RAM 0,KEIL RAM RAM

KEIL RAM

KEIL RAM



1	A/0			
